Lattice Semiconductor Corporation

PCB Layout Recommendations for BGA Packages

Introduction

As Ball Grid Array (BGA) packages become increasingly more popular, it is important to understand how they are affected by various board layout techniques. This document provides a brief overview of PCB layout considerations when working with BGA packages. It outlines some of the most common problems and provides tips for avoiding them at the design stage.

BGA Advantages

One of the greatest advantages of BGA packaging over other new technologies is that it can be supported with existing placement and assembly equipment. Most other new package types require new or upgraded processes, handlers and design methodologies. Incorporation of BGAs requires little more than a crash course in layout methodologies.

BGAs also offer significantly more misalignment tolerance, less susceptibility to coplanarity issues and easier PCB signal routing under a BGA package (see Figure 1).

BGA Disadvantages

The primary drawback of BGA packaging is the inability to access the solder joints for testing and inspection (a later section in this document provides layout recommendations for testing). At best, only the outermost row of balls can be seen, and board size and other components often restrict even that view. The best option available for a complete inspection of the device is an X-ray. By this means, the user can visually assess shorted connections, missing balls, filled vias, and in some cases opens (see Figure 2). Opens and partial opens (where the solder did not wet the entire pad) are more difficult to see and may require higher resolution equipment.

PCB Layout

Both types of pad layout, Solder Mask Defined and Non-Solder Mask Defined (SMD and NSMD respectively), have been successfully applied to BGA applications. Each layout type offers some advantages over the other and either may recommended, depending on the source.

Figure 1. Misalignment of BGA Balls vs. QFP Leads

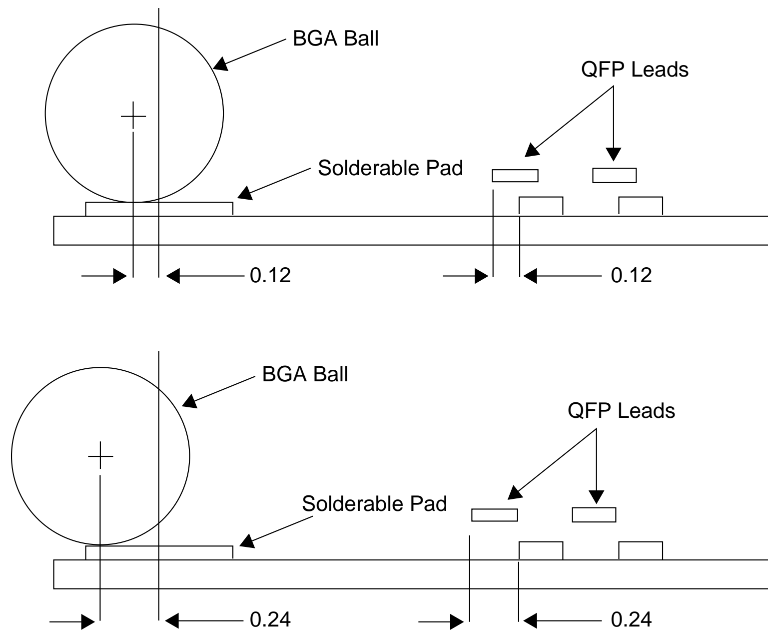
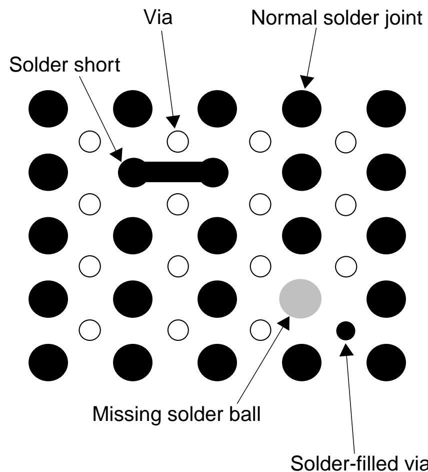


Figure 2. Example of How Defects May Appear in an X-Ray

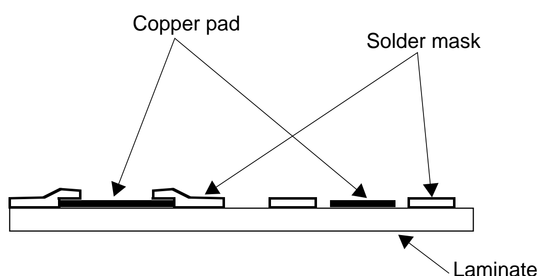


Solder Mask Defined Pads

In SMD pads, the solder mask comes up over the edge of the copper trace (see Figure 3). This adds an element of strength to the pad for two reasons. First, the solder mask overlap provides extra strength to the adhesion bond between the copper and the glass/epoxy laminate. Second, because the copper needs to extend beyond the edge of the solder mask, the actual copper area is larger. This provides additional copper surface to which the laminate can adhere. This added strength may be important in cases where the pad-to-PCB attachment could fail due to board flexing or excessive temperature testing.

Unfortunately, the larger copper area can also be a drawback since it leaves less space between pads for routing signal traces. While this is generally not a serious problem, it is more likely to occur when signals are assigned to pins that lay near the center of a large matrix BGA. Therefore, it is suggested to keep as many pin assignments as possible towards the periphery of the device.

Figure 3. SMD Pad (Left) and NSMD (Right)



Non-Solder Mask Defined Pads

In an NSMD pad the solder mask does not overlap the edge of the copper; thus the size of the copper defines the size of the pad. While this technique lacks some of the adhesion strength of the SMD pad, it can produce a more uniform hot air solder leveled surface finish and can leave more room between pads for signal routing.

The majority of BGA packages and designs use SMD type pads for added strength, however NSMD pads are gaining in popularity. Generally the best stress results come when the size of the PCB pad matches the size of the package pad. Be sure to check the specific pad information for the package being used.

Plated Through Hole Placement

Probably the most critical aspect of BGA PCB layout is the consideration for Plated Through Hole (PTH) placement. If the pad is too close or on top of the hole, or if there is no solder mask covering the via, then it is possible for the ball solder and paste to melt and be wicked into the hole. If enough solder is lost into the hole, the result could be an open for that lead. While this type of defect can usually be detected in an X-ray, it is best avoided at layout (see Figure 2).

Pad Geometries

Pad geometries (as shown in Figures 4 and 5) are typically circular. However, with a standard round pad, the X-ray of a soldered package looks the same regardless of the quality of wetting achieved; all that shows is the outline of the ball. By adding a slight variation in the shape of a dimple (Figure 6), it is possible to get a better X-ray view to check for opens. When the dimple feature is used, the solder wets to the entire pad surface and the ball deforms to the shape of the pad. This deformity is visible in an X-ray. The viewer must, however, learn to differentiate between a fully wet pad and one that simply has solder paste residue.

Layout Recommendations for Testability

Since it is impossible to probe BGA pins directly, PLD design and layout techniques that bring out several strategic pins as test points will allow testability of all of the internal PLD logic implementation.

This simple solution can be combined with the ispANALYZER™ software utility to provide full accessibility and testability to the PLD in a BGA package. The ispANALYZER lets the user bring out internal macrocells (or

Figure 4. NMSD Dogbone with Typical Dimenstions for Most 1.27mm Pitch PBGAs

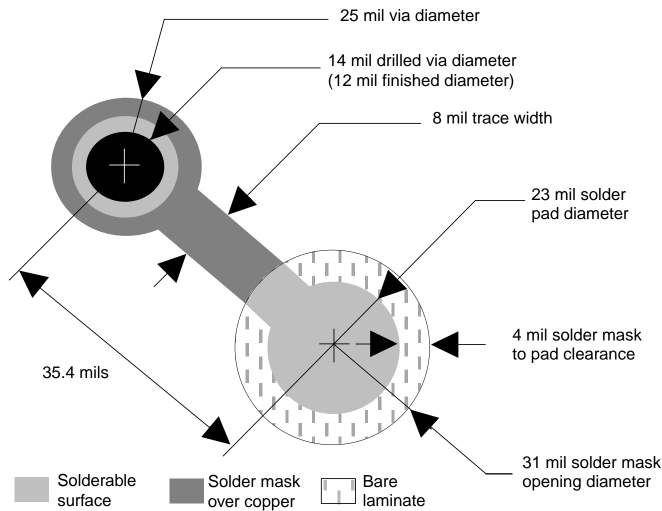
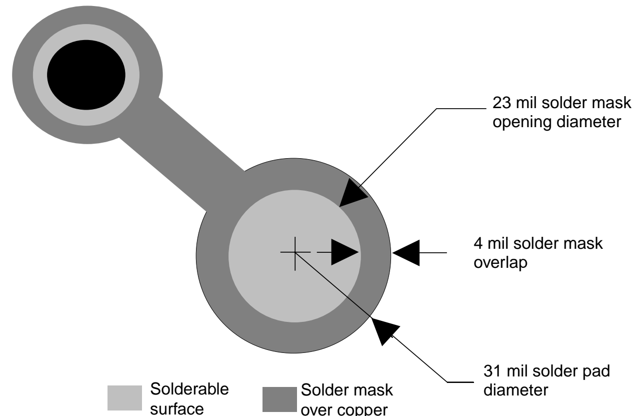


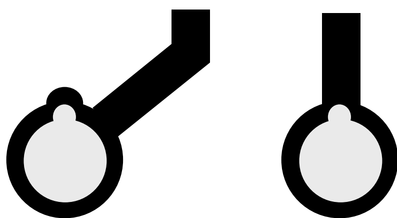
Figure 5. SMD Pad with Example Dimensions



other macrocell outputs) to unused I/O pins. With this capability, a suspect I/O pin can be tested via a test point that is designed to bring out a number of predefined I/O pins.

Another option is to make use of a Lattice ispGDX™ or ispGDS™ switch matrix device. These devices are designed to route signals, allowing the pinout of the BGA to change without affecting the layout of the board. By routing some or all of the BGA traces through a GDX you add complete flexibility to the pinout of the BGA device. The use of an ispGDX or ispGDS device can be especially powerful when used in conjunction with the ispANALYZER utility.

Figure 6. Examples of Solder Pad Bumps (Also Called Dimples or Ears)



For additional information on the Lattice ispGDX and ispGDS devices or the ispANALYZER software utility, contact your local Lattice sales office or Field Application Engineer, or visit the Lattice Semiconductor website at http:\\www.latticesemi.com.

Conclusion

Armed with a few simple layout tips, most of the difficulties in switching from QFP to BGA package use can be overcome. BGA packages are tolerant to misalignment and with the help of an X-ray machine it is easy to spot manufacturing defects and guarantee high PCB quality.