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ELECTRONICS INDUSTRIES®

IPC-7351A

Generic Requirements for Surface Mount Design and Land Pattern Standard

Developed by the Surface Mount Land Patterns Subcommittee (1-13) of the Printed Board Design Committee (1-10) of IPC

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Users of this publication are encouraged to participate in the development of future revisions.

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Generic Requirements for Surface Mount Design and Land Pattern Standard

1 SCOPE

This document provides information on land pattern geometries used for the surface attachment of electronic components. The intent of the information presented herein is to provide the appropriate size, shape and tolerance of surface mount land patterns to insure sufficient area for the appropriate solder fillet to meet the requirements of IPC J-STD-001, and also to allow for inspection, testing, and rework of those solder joints.

1.1 Purpose Although, in many instances, the land pattern geometries can be different based on the type of soldering used to attach the electronic part, wherever possible, land patterns are defined with consideration to the attachment process being used. Designers can use the information contained herein to establish standard configurations not only for manual designs but also for computer-aided design systems. Whether parts are mounted on one or both sides of the board, subjected to wave, reflow, or other type of soldering, the land pattern and part dimensions should be optimized to insure proper solder joint and inspection criteria.

Land patterns are dimensionally defined and are a part of the printed board circuitry geometry, as they are subject to the producibility levels and tolerances associated with plating, etching, assembly or other conditions. The producibility aspects also pertain to the use of solder mask and the registration required between the solder mask and the conductor patterns.

Note 1: The dimensions used for component descriptions have been extracted from standards developed by industrial and/or standards bodies. Designers should refer to these standards for additional or specific component package dimensions.

Note 2: For a comprehensive description of the given printed board and for achieving the best possible solder joints to the devices assembled, the whole set of design elements includes, beside the land pattern definition:

- Soldermask
- Solder paste stencil
- Clearance between adjacent components
- Clearance between bottom of component and printed board surface, if relevant
- Keepout areas, if relevant
- Suitable rules for adhesive applications

The whole of design elements is commonly defined as ‘‘mounting conditions.’’ This standard defines land patterns and includes recommendations for clearances between adjacent components and for other design elements.

Note 3: Elements of the mounting conditions, particularly the courtyard, given in this standard are related to the reflow soldering process. Adjustments for wave or other soldering processes, if applicable, have to be carried out by the user. This may also be relevant when solder alloys other than eutectic tin lead solders are used.

Note 4: This standard assumes that the land pattern follows the principle that, even under worst case conditions, the overlap of the component termination and the corresponding soldering land will be complete.

Note 5: Heat dissipation aspects have not been taken into account in this standard. Greater mass may require slower process speed to allow heat transfer.

Note 6: Heavier components (greater weight per land) require larger lands; thus, adding additional land pattern surface will increase surface area of molten solder to enhance capabilities of extra weight. In some cases the lands shown in the standard may not be large enough; in these cases, considering additional measures may be necessary.

1.2 Documentation Hierarchy This standard identifies the generic physical design principles involved in the creation of land patterns for surface mount components, and is supplemented by a shareware IPC-7351 Land Pattern viewer that provides, through the use of a graphical user interface, the individual component dimensions and corresponding land pattern recommendations based upon families of components. The IPC-7351 Land Pattern Viewer is provided on CD-ROM as part of this standard. Updates to land pattern dimensions, including patterns for new component families, can be found on the IPC website (www.ipc.org) under ‘‘PCB Tools and Calculators.’’ See Appendix C for more information on the IPC-7351 Land Pattern Viewer.

1.2.1 Component and Land Pattern Family Structure The IPC-7351 provides the following number designation within this standard for each major family of surface mount components to indicate similarities in solder joint engineering goals:

IPC-7352 – Discrete Components (CAP, RES, IND, DIO, LED)

IPC-7353 – Gullwing Leaded Components, Two Sides (SOP, SOIC, SOD, SOT, TO)