# AN10365

## Surface mount reflow soldering description

Rev. 02 — 26 July 2006 Application note

### Document information

| Info | Content |
|---|---|
| **Keywords** | surface mount reflow soldering |
| **Abstract** | This application note provides guidelines for the board mounting of IC packages. |

PHILIPS

## Revision history

| Rev | Date | Description |
|---|---|---|
| 02 | 20060726 | updates in Table 1, Table 8 and on page 20: the minimum peak reflow temperature when using SnPb solder is changed from 210 °C to 215 °C |
| 01 | 20050524 | initial version |

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# 1. Introduction

This application note provides guidelines for board mounting of surface mount IC packages. Nowadays, reflow soldering is a widely spread technology for soldering of surface mount IC packages. For some of the newer IC packages, such as Ball Grid Arrays (BGAs), reflow soldering is the only suitable method.

This application note describes the materials for reflow soldering: the Printed-Circuit Board (PCB), IC packages and solder paste. One of the key features of the PCB is the footprint design. The footprint design describes the recommended solder land on the PCB to make a reliable solder joint between the IC package and the PCB. A proven solder material is SnPb, but due to legislation the industry is changing to Pb-free solutions. Process requirements for solder paste printing and reflow soldering, for SnPb and Pb-free, are also discussed in this application note. This document concludes with a section about inspection and repair.

# 2. Materials

## 2.1 Printed-circuit boards and footprints

Printed-Circuit Boards (PCBs) are not only used as mechanical carriers for electronic components; they also provide the electronic interconnection between these components and also between these components and the outside world. These electronic components may be ICs, or other types such as capacitors and resistors. Through component selection and the use of Cu interconnections between the components, an electronic system, such as a mobile phone, can be assembled on a PCB. The substrates used for mounting the packages can be made of a variety of materials, including FR4 and flexible polymers.

Due to the increased transistor density in the latest IC technologies, generation of heat has become a major limitation of IC performance. By applying an exposed pad or heat sink in the IC package, in combination with thermal vias in the PCB, the heat can be transferred from the active die to the outside world. Four examples of vias capped in different ways, are shown in Figure 1. Note that the only difference lies in the solder resist pattern.

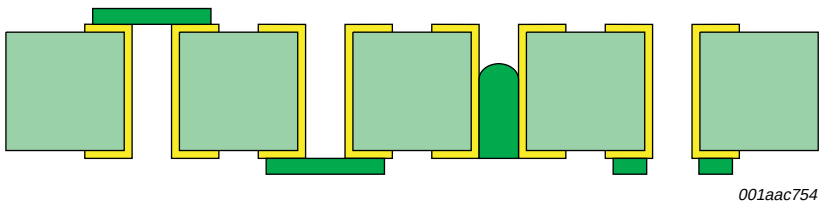


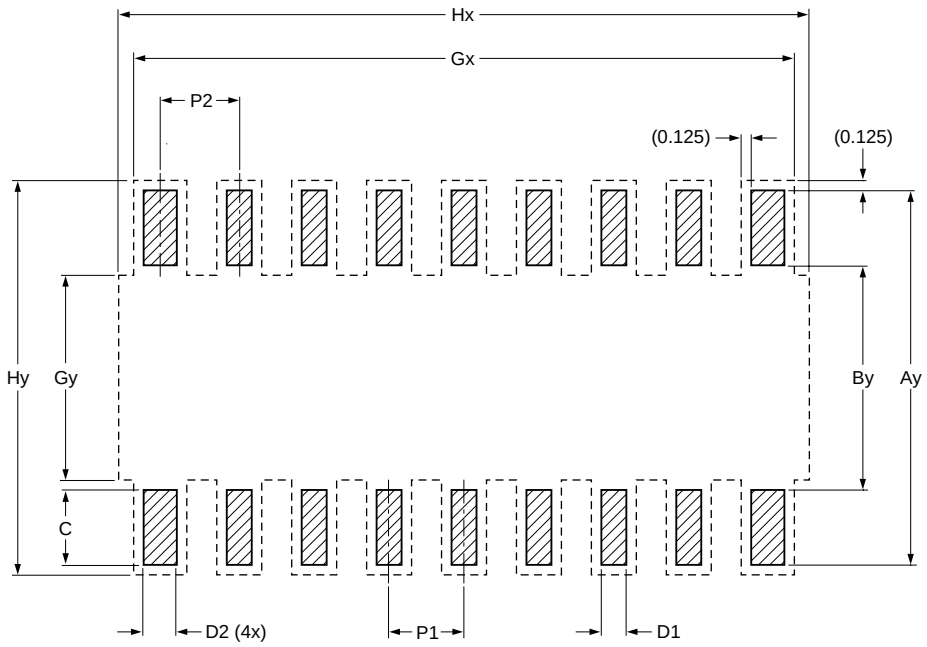

**Fig 1. Capped vias; from left to right: via tenting from top, via tenting from bottom, via capping from bottom, via encroached from bottom**

Common board finishes include NiAu, Organic Solderability Preservative (OSP), and SnAg. Although finishes may look different after reflow, and some appear to have better wetting characteristics than others, all common finishes can be used, provided that they are in accordance with the specifications.

Examples of other issues in board quality are tolerances on the pad and solder resist dimensions and component placement, maximum board dimensions, and flatness.

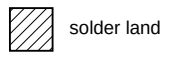
A footprint design describes the recommended dimensions of the solder lands on the PCB, to make reliable solder joints between the IC package and the PCB. The PCB footprints of Philips Semiconductors packages can be found by clicking ‘Package Information’ on the ‘Product Information’ page of the Philips Semiconductors web site at the URL given in “Contact information” at the bottom of page 2. The unique identifier for the PCB footprint is the Philips package outline code (the package SOT number). The next paragraph explains how to read the PCB footprint. Figure 2 shows an example of a PCB footprint, as found on the Philips Semiconductors web site.

**Footprint information for reflow soldering of SSOP20 package** **SOT266-1**




Generic footprint pattern

Refer to the package outline drawing for actual layout




**DIMENSIONS in mm**

| P1 | P2 | Ay | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|
| 0.650 | 0.750 | 7.200 | 4.500 | 1.350 | 0.400 | 0.600 | 6.900 | 5.300 | 7.300 | 7.450 |

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**Fig 2. PCB footprint for the SOT266-1 package (SSOP20)**

All footprints within a package family (in this example all SSOP packages) use the same generic footprint drawing, regardless of the actual number of package terminals. In this example, it is not accidental that the generic footprint drawing shows 18 terminals, whereas the SSOP20 package has 20 terminals. The table on the PCB footprint, below the drawing, shows the actual dimensions for the specific package outline (with 20 terminals), while the generic drawing is used to illustrate the dimensions. The real package outline (with the correct number of terminals) can be found under ‘Package information’ on the ‘Product information’ page of the Philips Semiconductors web site at the URL given in “Contact information” at the bottom of page 2.

The soldering process is carried out under a set of process parameters that includes accuracies in the process, and IC package, board, and stencil tolerances. The footprint design is directly related to these aspects of the soldering process; the calculation of these dimensions is based on process parameters that are compliant with modern machines and a state-of-the-art process.

A solder resist layer (also known as a solder mask layer) is usually applied to the board, to isolate the solder lands and tracks. If this solder resist extends onto the Cu, the remaining solderable area is solder resist defined. This is sometimes referred to as Solder Mask Defined (SMD). Figure 3 shows solder resist defined pads; yellow is Cu and dark green is solder resist. The Cu underneath the solder resist is shown in a lighter shade of green.

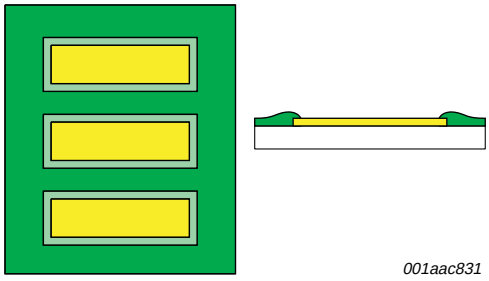


**Fig 3. Solder resist defined solder lands**

The alternative situation is that the solder resist layer starts outside of the Cu. In that case, the solder lands are Cu defined. This is sometimes referred to as Non Solder Mask Defined (NSMD). A Cu defined layout is shown in Figure 4 (white is the bare board).

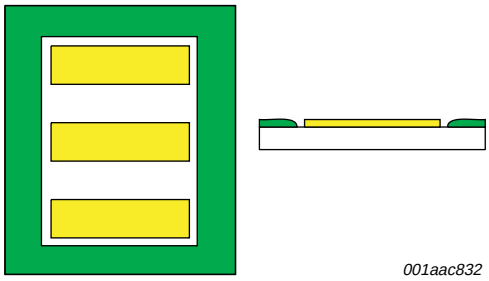


**Fig 4. Cu defined solder lands**

A layout may also be partially solder resist defined and partially Cu defined.

Note that a solder resist defined layout requires the application of a solder resist bridge between two terminals. There is a minimum width of solder resist that can be applied by board suppliers. This fact, in combination with a maximum solder resist placement accuracy, implies that solder resist defined layouts are not always possible. For IC packages with a small pitch, it is no longer possible to apply a solder resist bridge between two terminals, and a Cu defined or combination layout must be used.

If a solder land is solder resist defined, the Cu must extend far enough underneath the solder resist to allow for tolerances in Cu etching and solder resist placement during board production. Similarly, if a solder land is Cu defined, the solder resist must lie sufficiently far away from the solder land to prevent bleeding of the solder resist onto the Cu pad. Typical values for these distances are 50 μm to 75 μm.

The footprints referred to in this document indicate the areas that can be soldered.

The footprint shown in Figure 2 is redefined for both a solder resist and a Cu layout, in Figure 5. Note that the overlap/gap between the solder resist and the Cu is 0.05 mm in this particular example.

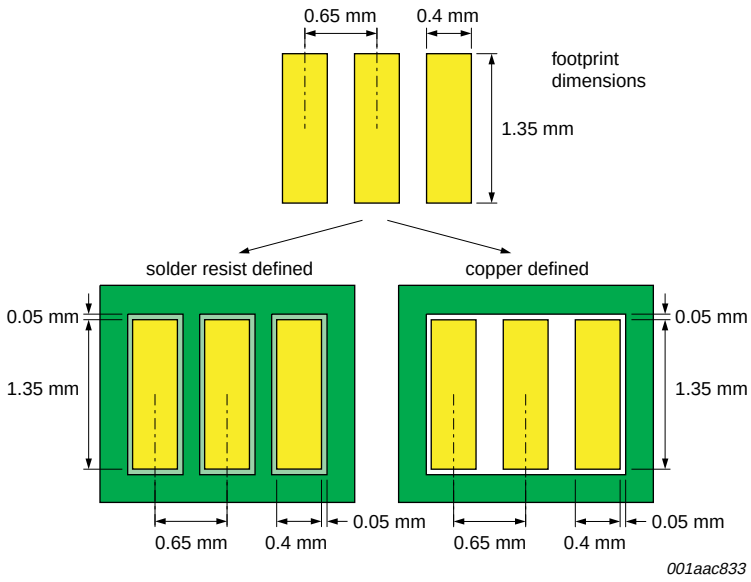


**Fig 5. Solder land dimensions for SOT266-1 package, either solder resist or Cu defined**

## 2.2 IC packages

IC packages may be divided into groups in various ways. In this document, they are categorized according to the shape of the terminals, as this has the largest influence on board assembly. Accordingly, the three main IC family types are the leaded packages (such as QFPs), the leadless packages with solder balls (such as BGAs) or leadless packages with solder lands (such as HVQFNs). Apart from the terminals, packages may have heat sinks and/or ground connections.

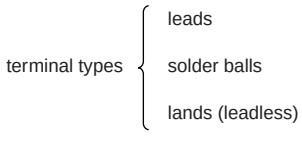


**Fig 6. Package types**

Leaded packages (e.g. SO and QFP)

- With leaded packages, coplanarity is an important issue; coplanarity must be within the specifications (refer to the package outline drawing) in order to prevent the occurrence of open circuits or bad joints; poor coplanarity may also increase problems caused by board warpage
- The tips of leads, where they are cut out of the leadframe, do not have to be wetted after reflow
- Possible lead finishes are SnPb, and pure Sn or NiPdAu for Pb-free applications
- Leaded packages are reflow solderable; standard gull wing packages are wave solderable, only if the lead pitch is equal or larger than 0.65 mm; wave soldering smaller pitches will lead to a higher defect level


**Fig 7. Example of a QFP**

Leadless packages with solder balls (e.g. BGA and TFBGA)

- These IC packages are particularly good at self-alignment, as the package body is essentially suspended over molten solder during reflow; therefore, this package type results in a robust reflow soldering process
- The balls are made of SnPb, or SAC for Pb-free applications
- Packages with solder balls are only reflow solderable, they cannot be wave soldered

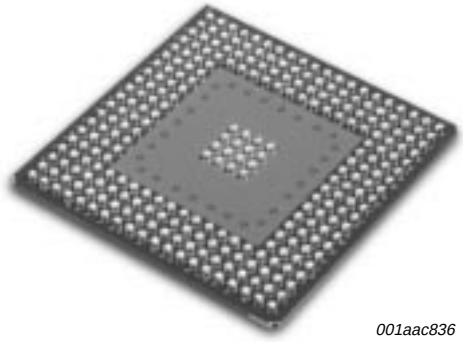

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**Fig 8. Example of a BGA**

Leadless packages with solder lands (e.g. HVQFN and HVSON)

- The exposed leadframe edges at the sides of the IC packages are often not finished - these do not have to be wetted for a proper joint
- Possible solder land finishes are SnPb, and pure Sn or NiPdAu for Pb-free applications
- Leadless packages with solder lands are reflow solderable only, they cannot be wave soldered

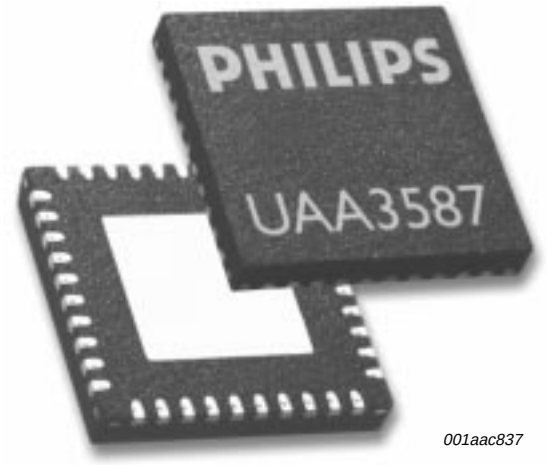


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**Fig 9. Example of an HVQFN**

IC packages may have heat sinks at the top or the bottom of the package. A few extra remarks are made on IC packages with heat sinks at the bottom (such as HVQFNs):

- Even if the exposed pad does not have to be soldered to the board for electrical or thermal purposes, the package reliability may improve if it is soldered to the board
- Voids in the solder joint connecting the heat sink pad to the board are allowed, provided that this does not conflict with demands made by the application

### 2.3 Solder paste

Solder that either contains Pb or which is Pb-free can be used, although it is advised to use Pb-free solder paste as this will be required by European legislation from July 2006 onward.

A wide variety of Pb-free solder pastes is available, containing combinations of tin, copper, antimony, silver, bismuth, indium, and other elements. The different types of Pb-free solder pastes have a wide range of melting temperatures. Solders with a high melting point may be more suitable for the automotive industry, whereas solders with a low melting point can be used for soldering consumer IC packages.

As a substitute for SnPb solder, the most common Pb-free paste is SAC, which is a combination of tin (Sn), silver (Ag), and copper (Cu). These three elements are usually in the range of 3 % to 4 % of Ag and 0 % to 1 % of Cu, which is near eutectic. SAC typically has a melting temperature of around 217 °C, and it requires a reflow temperature of more than 235 °C.

**Table 1. Typical solder paste characteristics**

| Solder | Melting temperature | Minimum peak reflow temperature |
|---|---|---|
| SnPb | 183 °C | 215 °C |
| SAC | 217 °C | 235 °C |

A no-clean solder paste does not require cleaning after reflow soldering and is therefore preferred, provided that this is possible within the process window. If a no-clean paste is used, flux residues may be visible on the board after reflow.

For more information on the solder paste, please contact your solder paste supplier.

## 3. Moisture sensitivity level and storage

If there is moisture trapped inside a package, and the package is exposed to a reflow temperature profile, the moisture may turn into steam, which expands rapidly. This may cause damage to the inside of the package (delamination), and it may even result in a cracked IC package body (the popcorn effect). A package's sensitivity to moisture, or Moisture Sensitivity Level (MSL), depends on the package characteristics and on the temperature it is exposed to during reflow soldering.

The MSL of IC packages can be determined through standardized tests in which the packages are moisturized to a predetermined level and then exposed to a temperature profile. Studies have shown that small and thin packages reach higher temperatures during reflow than do larger packages. Therefore, small and thin packages must be classified at higher reflow temperatures.

The temperatures that packages are exposed to are always measured at the top of the package body.

**Table 2. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)**

| Package thickness | Volume $mm^3 < 350$ | Volume $mm^3 \geq 350$ |
|---|---|---|
| < 2.5 mm | 240 °C + 0 °C/– 5 °C | 225 °C + 0 °C/– 5 °C |
| ≥ 2.5 mm | 225 °C + 0 °C/– 5 °C | 225 °C + 0 °C/– 5 °C |

**Table 3. Pb-free process - package classification reflow temperatures (from *J-STD-020C* July 2004)**

| Package thickness | Volume $mm^3$ < 350 | Volume $mm^3$ 350 to 2000 | Volume $mm^3$ > 2000 |
|---|---|---|---|
| < 1.6 mm | 260 °C + 0 °C | 260 °C + 0 °C | 260 °C + 0 °C |
| 1.6 mm to 2.5 mm | 260 °C + 0 °C | 250 °C + 0 °C | 245 °C + 0 °C |
| ≥ 2.5 mm | 250 °C + 0 °C | 245 °C + 0 °C | 245 °C + 0 °C |

The specified reflow profile is described in Table 4 and Figure 10. Note that this reflow profile is intended only for MSL testing and not for regular reflow soldering. This profile is the upper limit - above these temperatures, the package is not guaranteed.

**Table 4. MSL classification reflow profile - details (from *J-STD-020C* July 2004)**

| Profile Feature | SnPb eutectic assembly | Pb-free assembly |
|---|---|---|
| Average ramp-up rate ($Ts_{max}$ to Tp) | 3 °C/s maximum | 3 °C/s maximum |
| Preheat | | |
| Temperature minimum ($Ts_{min}$) | 100 °C | 150 °C |
| Temperature maximum ($Ts_{max}$) | 150 °C | 200 °C |
| Time $Ts_{min}$ to $Ts_{max}$ (ts) | 60 s to 120 s | 60 s to 180 s |
| Time maintained above | | |
| Temperature ($T_L$) | 183 °C | 217 °C |
| Time ($t_L$) | 60 s to 150 s | 60 s to 150 s |
| Peak/classification temperature (Tp) | see Table 2 | see Table 3 |
| Time within 5 °C of actual peak temperature ($t_p$) | 10 s to 30 s | 20 s to 40 s |
| Ramp-down rate | 6 °C/s maximum | 6 °C/s maximum |
| Time 25 °C ($t_{25°C}$) to peak temperature | 6 minutes maximum | 8 minutes maximum |

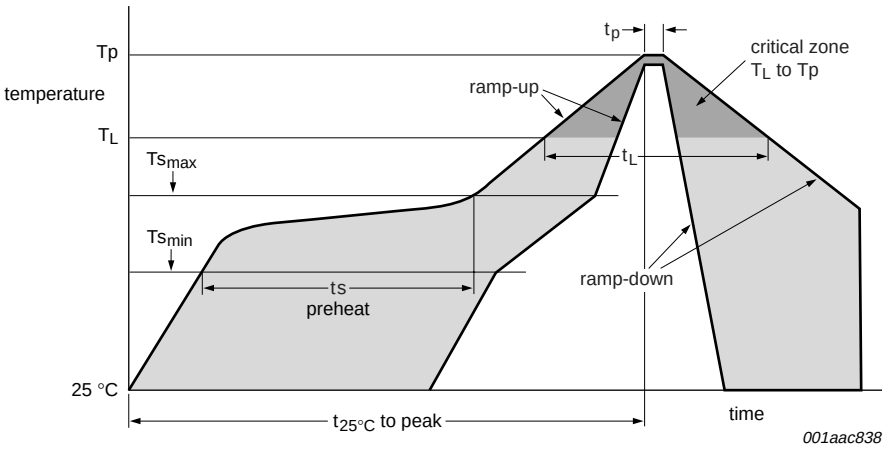



**Fig 10. MSL classification reflow profile (from *J-STD-020C* July 2004)**

Depending on the damage after this test, an MSL of 1 (not sensitive to moisture) to 6 (very sensitive to moisture) is attached to the IC package. For every product, this MSL is given on a packing label on the shipping box. Each package is rated at two temperatures, for SnPb and Pb-free soldering conditions. An example of a packing label is given in Figure 11.


**Fig 11. Example of MSL information on sticker; note the two MSLs, corresponding to the two reflow processes**

An MSL corresponds to a certain out-of-bag time (or floor life). If IC packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow, in order to remove any moisture that might have soaked into the package. MSLs and temperatures on the package bag labels are to be respected at all times. Naturally, this also means that IC packages with a critical MSL may not remain on the placement machine between assembly runs.

The IC package floor life, as a function of the MSL, can be found in Table 5.

**Table 5. Floor life as a function of MSL**

| MSL | Floor life | |
|---|---|---|
| | Time | Conditions |
| 1 | unlimited | ≤ 30 °C/85 % RH |
| 2 | 1 year | ≤ 30 °C/60 % RH |
| 2a | 4 weeks | ≤ 30 °C/60 % RH |
| 3 | 168 hours | ≤ 30 °C/60 % RH |
| 4 | 72 hours | ≤ 30 °C/60 % RH |
| 5 | 48 hours | ≤ 30 °C/60 % RH |
| 5a | 24 hours | ≤ 30 °C/60 % RH |
| 6 | 6 hours | ≤ 30 °C/60 % RH |

# 4. Surface mounting process

## 4.1 Solder paste printing

Solder paste printing requires a stencil aperture to be completely filled with paste. Then, when the board is released from the stencil, the solder paste is supposed to adhere to the board, so that all of the paste is released from the stencil aperture, and a good solder paste deposit remains on the board. Ideally, the volume of solder paste on the board should equal the ‘volume’ of the stencil aperture.

In practice, however, not all of the solder paste is released from the stencil aperture. The percentage of paste release depends largely on the aperture dimensions, i.e. the length and width and the depth (the stencil thickness). If a stencil aperture becomes very small, the paste will no longer release completely. Furthermore, stencil apertures must be larger if a thicker stencil is used.

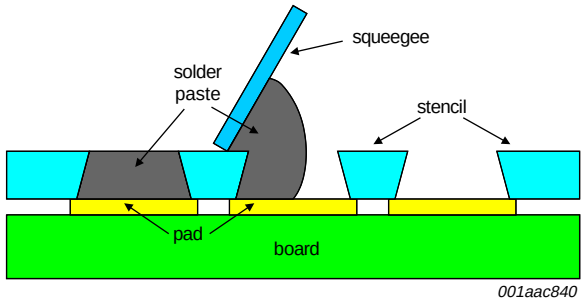



**Fig 12. Stencil printing**

Another important factor is the aperture shape, i.e. whether the aperture is rectangular, trapezoidal, or otherwise. Paste release also depends - amongst others - on the loading and speed of the squeegee, the board separation speed, the printing direction, and the aperture orientation. In essence, all of these parameters must be adjusted so that all solder paste deposits on one board, from the smallest to the largest, are printed properly.

Consequences of insufficient solder paste printing are usually open contacts or bad joints. These may arise because:

- The solder paste deposit is not sufficiently high: components or their leads may not make proper contact with the paste, resulting in open circuits or bad joints, or
- There is insufficient solder volume for a proper solder joint, also resulting in open circuits, or
- The activator is used up rapidly in a small solder paste deposit, so that the paste no longer properly wets the component metallization, also resulting in open circuits

A second important aspect in solder paste printing is smearing. If some solder paste bleeds between the stencil and the board during one printing stroke, then the next board may not fit tightly to the stencil, allowing more paste to bleed onto the bottom of the stencil. Once this effect starts, it strengthens itself. As a result, the solder paste may eventually form bridges that stretch from one paste deposit to the next. If a bridge is

narrow enough, it will snap open during reflow, as the volume of molten solder seeks to attain minimum surface area. A wider bridge, however, may remain stable, resulting in a short-circuit.

To achieve a difference in solder paste volumes on one board, it is possible to use a stencil that has a different thickness at different locations. An example of this is the step-stencil. This, however, is only recommended if there is no other solution.

Stencils are commonly made from Nickel; they may be either electro formed or laser-cut. Typical stencil thicknesses are given in Table 6.

**Table 6. Typical stencil thicknesses**

| IC package pitch | Stencil thickness |
|---|---|
| ≥ 0.5 mm | 150 µm |
| 0.4 mm to 0.5 mm | 125 µm |

Except for BGAs, no stencil aperture dimensions are given with the footprints in this document. However, a general rule is that the stencil apertures must be 25 µm smaller than the solder lands, on all sides. In other words, the solder paste lies 25 µm inward from the solder land edge. This usually results in stencil aperture dimensions that are 50 µm smaller than the corresponding solder land dimensions; see Figure 13.

This rule does not apply for BGAs; for BGAs the solder paste deposit is shown explicitly in the PCB footprint specification. Although BGA balls and their solder pads are circular, square stencil apertures are sometimes preferred for BGAs.

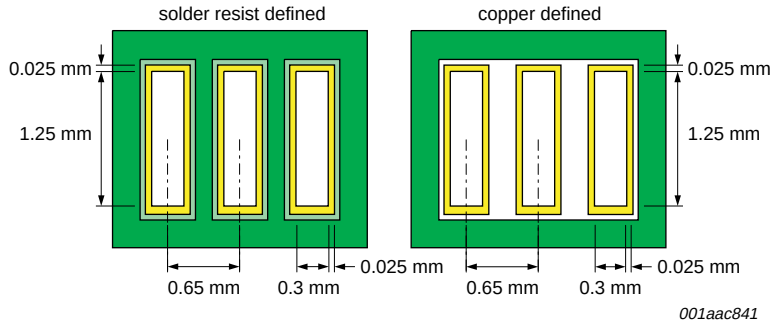



**Fig 13. Solder paste printing on solder and capped resist defined layouts**

Another exception lies with the very large solder lands, such as when printing solder paste on a heat sink land. In that case, it is advised to print an array of smaller solder paste deposits. The solder paste should cover approximately 20 % of the total land area. It is also advised to keep the solder paste away from the edges of this land: the solder paste pattern, including the spacing between the deposits, should have a coverage of 35 % of the land area; see Figure 14 and 15.

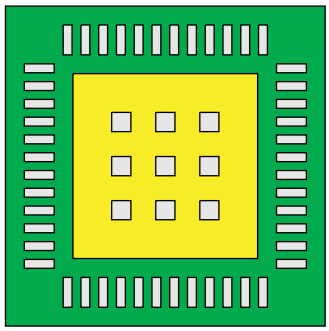



Fig 14. Paste coverage

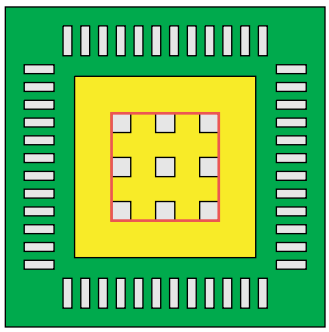



Fig 15. Pattern coverage

The paste printing pattern for exposed die pads is illustrated with an example, see Figure 16. A HVQFN48 with an exposed pad of 5.1 mm × 5.1 mm, for example, should have nine solder paste deposits that are arranged in a three-by-three array. The solder paste deposits are 0.76 mm × 0.76 mm, and the distance between them is 0.37 mm.

This way, the solder paste area is $9 \times 0.76^2$ mm$^2$, and dividing this by the land area ($5.1^2$ mm$^2$) yields a solder paste coverage of approximately 20 %.

Similarly, the solder paste pattern (the paste, plus the area between the deposits) has a length of 3.02 mm. The pattern area, $3.02^2$ mm$^2$, divided by the land area, yields a paste pattern coverage of approximately 35 %.

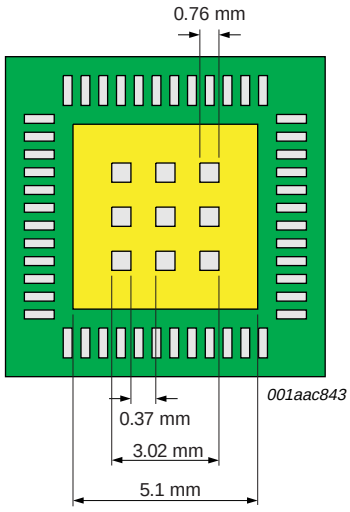



Fig 16. Solder paste dimensions on the land area for an exposed die pad of HVQFN48

Depending on the solder paste used, the solder paste deposits printed on a large land may not always coalesce completely. In some cases, individual solder joints can still be recognized between the exposed die pad and solder land on the board. It is possible that voids remain in the solder joints. Whether or not voids or incomplete coalescing of the solder are a problem, depends on the application. For low-power devices in which little heat is generated, up to 80 % of voids may still be acceptable.

Keep in mind that printing a smaller volume of solder paste could have adverse effects on the solder joint reliability. Also, if there are vias in pads, solder paste deposits should be arranged so that paste is never printed directly over a via.

## 4.2 IC package placement

The required placement accuracy of a package depends on a variety of factors, such as package size and the terminal pitch, but also the package type itself. During reflow, when the solder is molten, a package that has not been placed perfectly may center itself on the pads: this is referred to as self-alignment. Therefore, the required placement accuracy of a package may be less tight if this package is a trusted self-aligner. It is known, for example, that BGAs are good at self-alignment, as the package body essentially rests on a number of droplets of molten solder, resulting in minimal friction.

Typical placement tolerances, as a function of the IC package terminal pitch, are given in Table 7.

**Table 7. Typical placement accuracies**

| Package terminal pitch | Placement tolerance |
|---|---|
| ≥ 0.65 mm | 100 μm |
| < 0.65 mm | 50 μm |

IC packages are usually placed with two types of machines. If the highest placement accuracy is required, the slower but more accurate machines must be used. These machines are also often more flexible when it comes to unusual package shapes, that may require dedicated nozzles and non-standard trays. If the highest placement accuracy is not necessary, and there are no special requirements, fast component mounters, or chip shooters, can be used. These machines can process up to 100,000 components per hour.

The placement force may also be an important parameter for some packages. In theory, an IC package is always pressed down into the solder paste until it rests on a single layer of solder paste powder particles - the rest of the solder paste is pressed aside. A consequence that is immediately apparent, is that the solder paste that is pushed aside, or that bulges outside the package, may cause bridges with neighboring solder paste deposits.

In extreme cases, solder paste may not only bulge outside the pads, but it may actually be blasted further away from the pads, so that a small amount of solder paste is no longer connected to the paste deposit it originally came from. This must always be avoided, as the splattered solder paste may cause shorts elsewhere on the board, and the solder paste deposit it originally came from may end up with insufficient solder. Incidentally, this effect is often caused in part by use of an improper nozzle shape, so that the paste is actually blown away by air from the nozzle.

If the placement force is too low, there is a chance that an IC package terminal does not make sufficient contact with the solder paste. In that case, there is a risk that the solder paste tackiness will not be able to hold it in place up to the reflow zone in the oven, and the package may be displaced. In addition, even if the IC package remains in place, there may be bad contact between the package terminals and the solder paste, resulting in open contacts or bad joints.

Therefore, the placement force must always be adjusted so that there is no excessive paste bulging or even splattering and there is a proper contact between the IC package and the solder paste. The necessary placement force to achieve this will depend on a number of factors, including the package dimensions. Typical forces are 2 N to 4 N. Note, however, that some of the more modern machines have a sensor that detects the package's proximity to the solder paste, so that the placement speed is reduced as soon as the package comes near to, or touches, the solder paste. In this way, splattering can be minimized.

## 4.3 Reflow soldering

The most important step in reflow soldering is reflow itself, when the solder paste deposits melt and soldered joints are formed. This is achieved by passing the boards through an oven, and exposing them to a temperature profile that varies in time.

A temperature profile essentially consists of three phases:

1. Preheat: the board is warmed up to a temperature that is lower than the melting point of the solder alloy
2. Reflow: the board is heated to a peak temperature that is well above the melting point of the solder, but below the temperature at which the components and boards are damaged
3. Cooling down: the board is cooled down rapidly, so that soldered joints freeze before the board exits the oven

The peak temperature during reflow has an upper and a lower limit:

1. Lower limit of peak temperature; the minimum peak temperature must be at least high enough for the solder to make reliable solder joints; this is determined by solder paste characteristics; contact your paste supplier for details
2. Upper limit of peak temperature; the maximum peak temperature must be lower than:
   a. The test temperature used for MSL assessment; see Section 3 "Moisture sensitivity level and storage".
   b. The temperature at which the boards are damaged; this is a board characteristic; contact your board supplier for details.

A rough indication of the recommended minimum peak temperatures for SnPb and SAC alloys is given in Table 8; however, these values should be verified with your solder paste supplier.

**Table 8. Typical solder paste characteristics**

| Solder | Melting temperature | Minimum peak reflow temperature |
|---|---|---|
| SnPb | 183 °C | 215 °C |
| SAC | 217 °C | 235 °C |

When a board is exposed to the profile temperature, certain areas on the board will become hotter than others: a board has hot spots (the hottest areas) and cold spots (the coolest areas). Cold spots are usually found in sections of the board that hold a high density of large components, as these soak up a lot of heat. Large areas of Cu in a board will also reduce the local temperature. Hot spots, on the other hand, are found in areas

with few components, or only the smallest components, and with little Cu. Finally, the board dimensions, and the board orientation in the oven, may also affect the location of hot and cold spots.

The temperature of the hot spot on a board must be lower than the upper limit of the peak temperature. Similarly, the temperature of the cold spot must be higher than the lower limit of the peak temperature.

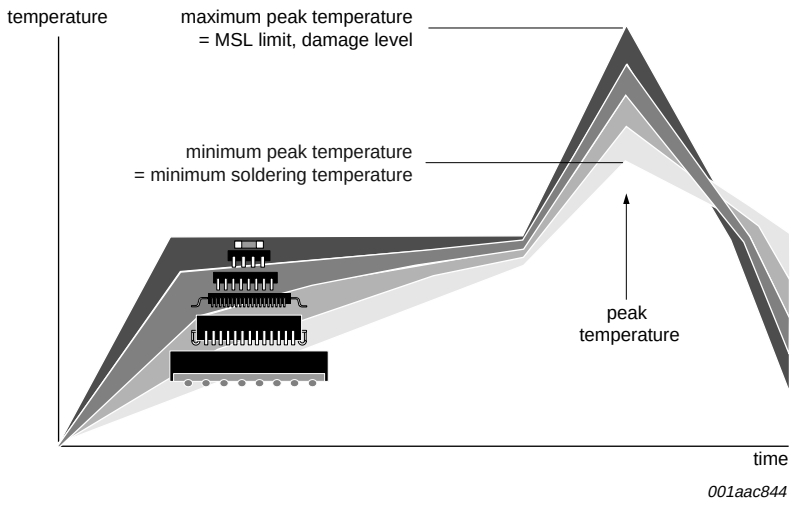



**Fig 17. Temperature profiles for large and small components**

In Figure 17, the grey band with the large component represents cold spots, and the dark band, at the top, with the smallest component, represents hot spots. In both cases, the graph first represents a component body temperature, measured at the top of the body. In the preheat phase, the hot spots will heat up rapidly to a temperature lower than the melting point of the solder alloy. They may remain at this temperature for a while. Note, however, that small solder paste deposits should not remain at an intermediate temperature for so long that their activator runs out: for small solder paste deposits, a fast temperature profile is preferred. The cold spots on the board will warm up far more slowly. The oven settings should be planned so that the cold as well as the hot spots will have reached roughly the same temperature by the end of the preheat phase.

The second phase in the reflow profile is the reflow zone, in which the solder melts and forms soldered joints. The minimum peak temperature, which all solder joints in the cold as well as the hot spots must reach, depends on the solder alloy. However, no region on the board may surpass a maximum peak temperature, as this would result in component and/or board damage. See Section 3 “Moisture sensitivity level and storage” for more information. Even if the cold and hot spots at the start of the reflow phase have roughly the same temperature, the hot spots will reach a higher peak temperature than the cold spots. Yet, both the hot spots and the cold spots must lie within the allowed peak temperature range. This may require some tweaking of the oven temperature settings and conveyor belt speeds. In some cases, the board layout may have to be optimized to limit the temperature difference between the cold and the hot spots.

When reflow soldering, the peak temperature should never exceed the temperature at which either the components or the board are damaged. The maximum peak temperature for components is partially determined by their moisture sensitivity. For reflow soldering

with SnPb solder, the peak temperature should be higher than 215 °C; when soldering with SAC, the peak temperature should be higher than 235 °C. Note that this usually implies a smaller process window for Pb-free soldering, thus requiring tighter process control.

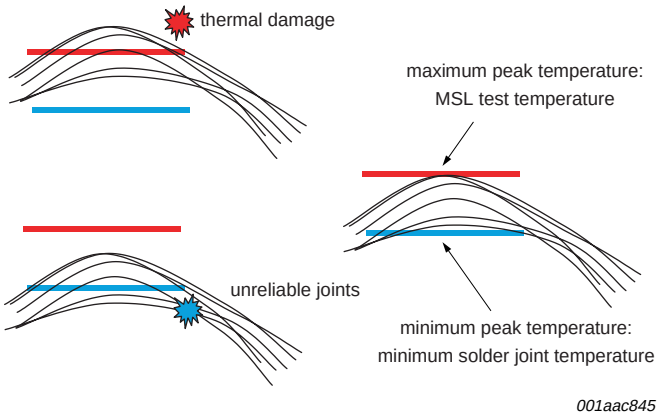



**Fig 18. Fitting both the hot and cold spots into the required peak temperature range**

The black lines in Figure 18 represent the actual temperature profiles for a number of different spots on a board. The bottom black line represents the coldest spot, and the top black line represents the hottest spot. The blue line represents the minimum peak temperature, and the red line is the maximum peak temperature. At the top left, some regions on the board are exposed to temperatures that are too high, exceeding MSL qualification conditions. At the bottom left, some regions on the board are exposed to temperatures that are too low, resulting in unreliable joints. At the right, all of the regions on the board have peak temperatures that fall within the upper and lower limits.

Reflow may be done either in air or in nitrogen. In general, nitrogen should not be necessary; in that case, air is preferred because of the lower cost. Reflow may be done in convection reflow ovens, some of which have additional infrared heating. Furthermore, using vapour phase reflow soldering can reduce temperature differences on a board.

## 4.4 Solder and terminal finish or solder ball compatibility

In selecting a solder paste, care must be taken that the solder is compatible with both the board and the IC package finishes. When soldering leaded or leadless packages, all package finishes may be freely combined with all solders; see Table 9.

**Table 9. Compatibility of ball and solder paste alloys, for leaded or leadless packages**

| Terminal finish | SnPb solder | Pb-free solder |
|---|---|---|
| SnPb | mature technology | OK |
| Pb-free | OK | OK |

This, however, is not the case for packages with solder balls. If these packages are soldered, the IC package solder balls and the solder paste both melt, to form a single joint. Therefore, it is essential that the reflow temperature profile reaches a temperature that is high enough for both the solder paste and the solder ball to melt and to form proper solder joints.

SnPb needs a temperature of at least 215 °C, but at least 235 °C is required for most Pb-free solders. There are four options:

- SnPb balls are combined with a SnPb paste; the balls and paste form good joints at a temperature of 215 °C or more; this combination has been used for decades
- SnPb balls are combined with a Pb-free paste; the paste requires a higher reflow temperature of at least 235 °C; the solder balls only need 215 °C, so they will also melt properly: OK
- Pb-free solder balls are combined with a SnPb paste; in this case, only the Pb-free balls require a higher reflow temperature, whereas the rest of the process does not; therefore, this combination is not advised
- Pb-free solder balls are combined with a Pb-free paste; now the paste requires the same reflow temperature, and so do the solder balls: OK

The text above is summarized in Table 10.

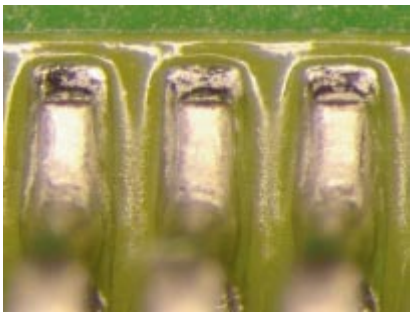
**Table 10. Compatibility of ball and solder paste alloys, for packages with solder balls**

| Solder ball | SnPb solder | Pb-free solder |
|---|---|---|
| SnPb balls | mature technology | OK |
| Pb-free balls | not advised | OK |

# 5. Inspection and repair

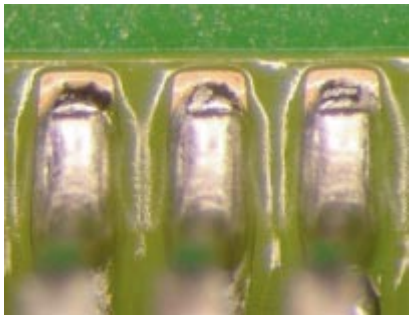
## 5.1 Inspection

In general, Pb-free solder is a little less successful at wetting than SnPb solders; SAC fillets will have a larger contact angle between the fillet and the wetted surface. When using Pb-free solder, this contact angle may typically be 20° to 30°. Notice the difference between SnPb and Pb-free solder in Figure 19: in the photograph on the left (SnPb), the solder lands have been wetted completely. In the photograph on the right, however, the solder has left part of the solder lands unwetted.



001aac846

a. SnPb solder joints

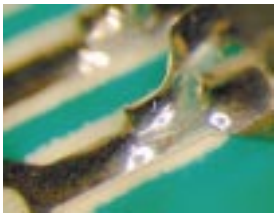


001aac863

b. Pb-free solder joints

**Fig 19. Difference in wetting between SnPb and Pb-free solder joints**

Another visual aspect in Pb-free soldering is that Pb-free solder joints tend to be less shiny than SnPb solder joints, and they may have striation marks. This is due to the different microstructure that is formed during solidification. Although SnPb solder joints should be rejected if they look this way, this is normal for Pb-free, and no reason to reject Pb-free solder joints.



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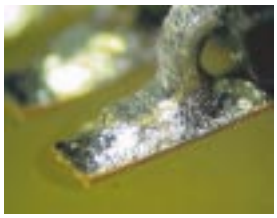
a. SnPb solder joints



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b. Pb-free solder joints

**Fig 20. Difference in appearance between SnPb and Pb-free solder joints**

## 5.2 Repair

Sometimes, a package lead that has not been soldered properly may be repaired simply by heating this single lead with the tip of a soldering iron. In that case, it is sufficient to heat the lead until the solder melts completely, and a new device should not be necessary.

In other situations, however, there may be a need to replace an IC package on the board. In that case, the rework process should consist of the following steps:

1. Device removal
2. Site preparation
3. Application of solder paste to the site
4. Device placement
5. Device attachment

It is advised to dry bake the board for 4 hours at 125 °C, prior to steps 1 to 5.

### 5.2.1 Device removal

In order to remove an IC package from the board, it must be heated; if possible, this must be done as locally as possible, to avoid heating the surrounding board and components. Packages with leads at a relatively large pitch may first be removed from the board by cutting the leads, after which only the leads must be de-soldered. This can be done with a soldering iron.

IC packages without leads must be heated entirely, for removal. Heat can be supplied using a hot air gun, a soldering iron, or focused infrared energy, depending on the package type and availability. If necessary, the bottom of the board can also be heated. The temperature to which the package solder joints should be heated depends on the solder that was originally used, and it is best to keep the temperature as low as possible, just above the melting point of the solder alloy used.

As soon as the solder has melted, the IC package is lifted from the board using a vacuum wand or tweezers; note that package removal should not be initiated until the solder has melted entirely.

Re-use of removed IC packages is not recommended.

### 5.2.2 Site preparation

After the device has been removed, the board area must be prepared for the new device. Prepare the site by removing any excess solder and/or flux remains from the board. Ideally this can be done on an appropriate de-soldering station, using solder wick or an alternative method.

After most of the solder has been removed from a solder land, a very thin layer of solder will be left, on top of a few intermetallic layers. In the case of Cu boards, for example, there will be layers of $Cu_3Sn$, $Cu_6Sn_5$, and finally solder, on top of the Cu. The top layer of solder is easily solderable.

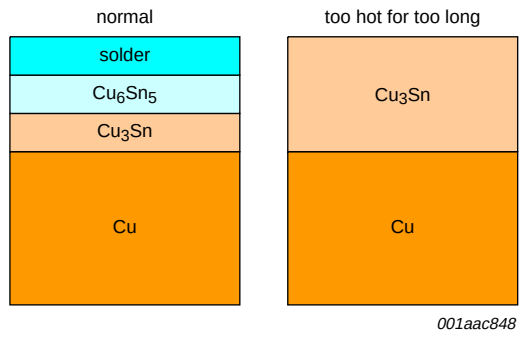


**Fig 21. Overheating and $Cu_3Sn$ formation**

If, however, the pad is heated too much during removal of the rejected IC package, and during site preparation, the top two layers will also be converted into $Cu_3Sn$; in that case, there will only be the $Cu_3Sn$ intermetallic layer on top of the Cu. Unfortunately, $Cu_3Sn$ is hardly wettable. As a result, it will become very difficult to solder the replacement package at this location. Therefore, care must be taken during reject package removal and site redress, that the solder lands are heated not more than necessary.

### 5.2.3 Solder paste printing

After the site redress is completed, solder paste should be applied to either the site or the device. This can be done by using a miniature stencil or other in-house techniques. Preferably, the same type of solder paste should be used as was originally applied on the board.

If the new device that is to be soldered to the board has solder balls, solder paste printing is not necessary. In that case it suffices to apply a thin layer of tacky flux on the solder lands on the PCB.

### 5.2.4 Device placement

The last step of the repair process is to solder the new IC package on the board. If necessary, the new package may be aligned under a microscope or split beam system, possibly in a special repair station. If this is not possible, try to align the device with board markers.

### 5.2.5 Soldering

To reflow the solder, apply a temperature profile that is as close as possible to the original reflow profile used for assembling the board. Take care that the board and/or IC package are not moved or tilted until the solder has solidified completely. Note that if a board is exposed to reflow temperatures a second time, it may be necessary to dry bake the board for the sake of the components that have already been mounted.

## 6. References

[1] **IPC/JEDEC J-STD-020C July 2004 —** Joint Industry Standard Moisture/Reflow, Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

# 7. Legal information

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**Date of release: 26 July 2006**

**Document identifier: AN10365_2**